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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/522,572	01/28/2005	Kun-Hong Lee	LEEK3013/REF	8793

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EXAMINER	
QUARTERMAN, KEVIN J	

ART UNIT	PAPER NUMBER
2889	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/522,572	LEE ET AL.	
	Examiner	Art Unit	
	Kevin Quarterman	2889	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 January 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1107*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment and remarks received 04 January 2008 have been entered and overcome the objections to the claims.

Drawings

2. The replacement-drawings were received on 04 January 2008. These drawings are acceptable.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-39 are rejected under 35 U.S.C. 102(b) as being anticipated by Cho (KR 10-2002-0041665).

5. Regarding independent claim 1, the figures of Cho show an electric field emission device having a triode structure fabricated using an anodic oxidation process comprising a supporting substrate (10); a bottom electrode layer (11) formed on the supporting substrate, which is used as a cathode electrode of the device; a gate insulating layer (12) formed on the bottom electrode layer, the gate insulating layer having a plurality of first sub-micro holes (25) to be used as gate holes of the device; a gate electrode layer (13) formed on the gate insulating layer, the gate electrode layer

having a plurality of second sub-micro holes each connecting to a corresponding one of the first sub-micro holes; an alumina layer (15) formed on the gate electrode layer, the alumina layer having a plurality of third sub-micro holes each connecting to a corresponding one of the second sub-micro holes; a top electrode layer (Fig. 8) for hermetically sealing the device in a vacuum, which is formed on the alumina layer and used as an anode of the device; and a plurality of emitters (23) for emitting electrons in a high electric field, each of the emitters being formed in a corresponding one of the first sub-micro holes.

6. Regarding claim 2, Cho discloses the emitter containing metal, semiconductor, or carbon material.

7. Regarding claim 3, Cho discloses the carbon material being selected from a group consisting of a carbon nano-fiber, a carbon nano-tube, a carbon nano-particle, and amorphous carbon material.

8. Regarding claim 4, Figure 7 of Cho shows a resistive layer (19) formed between the bottom electrode and the gate insulating layer.

9. Regarding claim 5, Cho discloses the resistive layer containing SiO_2 or metallic oxide.

10. Regarding independent claim 6, the figures of Cho show an electric field emission device having a triode structure fabricated using an anodic oxidation process comprising a supporting substrate (10); a bottom electrode layer (11) formed on the supporting substrate, which is used as a cathode electrode of the device; a gate insulating layer (12) formed on the bottom electrode layer, the gate insulating layer

having a plurality of first sub-micro holes (25) to be used as gate holes of the device; a gate electrode layer (13) formed on the gate insulating layer, the gate electrode layer having a plurality of second sub-micro holes each connecting to a corresponding one of the first sub-micro holes; an anode insulating layer (15) formed on the gate electrode layer, having a plurality of third sub-micro holes each connecting to a corresponding one of the second sub-micro holes; a top electrode layer (Fig. 8) for hermetically sealing the device in a vacuum, which is formed on the anode insulating layer and used as an anode of the device; and a plurality of emitters (23) for emitting electrons in a high electric field, each of the emitters being formed in a corresponding one of the first sub-micro holes.

11. Regarding claim 7, Cho discloses the emitter containing metal, semiconductor, or carbon material.

12. Regarding claim 8, Cho discloses the carbon material being selected from a group consisting of a carbon nano-fiber, a carbon nano-tube, a carbon nano-particle, and amorphous carbon material.

13. Regarding claim 9, Figure 7 of Cho shows a resistive layer (19) formed between the bottom electrode and the gate insulating layer.

14. Regarding claim 10, Cho discloses the resistive layer containing SiO_2 or metallic oxide.

15. Regarding independent claim 11, Figures 1-8 of Cho show a method for fabricating an electric field emission device having a triode structure by using an anodic oxidation process comprising the steps of forming a bottom electrode (11) on a

supporting substrate (10), the bottom electrode layer being used as a cathode electrode of the device; forming sequentially a gate insulating layer (12), a gate electrode layer (13), and an aluminum layer (15) on the bottom electrode layer; forming a plurality of first sub-micro holes in an alumina layer by performing an anodic oxidation process on the aluminum layer, thereby transforming the aluminum layer into the alumina layer; etching a barrier layer of the alumina layer and the gate electrode layer, thereby a surface of the gate insulating layer being exposed through the first sub-micro holes; forming a plurality of second sub-micro holes in the gate insulating layer, thereby each of the first sub-micro holes connecting to a corresponding one of the second sub-micro holes; forming an emitter (23) for emitting electrons in a high electric field in each of the second sub-micro holes; and forming a top electrode layer (Fig. 8) for hermetically sealing the device on the alumina layer in a vacuum, the top electrode layer being used as an anode of the device.

16. Regarding claim 12, Cho discloses the anodic oxidation process being performed by using an electrolyte selected from a group consisting of oxalic acid, sulfuric acid, phosphoric acid, and chromic acid.

17. Regarding claim 13, Cho discloses the barrier layer of the alumina layer and the gate electrode layer being etched by using one of ion milling, dry etching, and wet etching techniques.

18. Regarding claim 14, Cho discloses the gate insulating layer being etched by using one of ion milling, dry etching, wet etching, and anodic oxidation techniques.

19. Regarding claim 15, Cho discloses each of the emitters being formed by growing metal from a bottom of each of the second sub-micro holes.

20. Regarding claim 16, Cho discloses the metal being grown by applying DC or AC voltage or voltage pulse to a solution of metal sulfate, metal nitrate, or metal chloride.

21. Regarding claim 17, Cho discloses the metal being grown by using a solution of metal sulfate, metal nitrate, or metal chloride after chemically activating a surface of the bottom.

22. Regarding claim 18, Cho discloses each of the emitters being formed by attaching a metal to a bottom of each of the second sub-micro holes.

23. Regarding claim 19, Cho discloses each of the emitters being formed by forming a carbon nano-structure on a bottom of each of the second sub-micro holes.

24. Regarding claim 20, Cho discloses the carbon nano-structure being one of carbon nano-tube, carbon nano-fiber, amorphous carbon, and carbon nano-particle, which are composed by using a thermal decomposition.

25. Regarding claim 21, Cho discloses the thermal decomposition being performed by thermally decomposing a gas mixture of hydrocarbon, carbon monoxide, and hydrogen at 200-800°C.

26. Regarding claim 22, Cho discloses the carbon nano-structure being one of carbon nano-tube, carbon nano-fiber, amorphous carbon, and carbon nano-particle, which are composed by using a plasma decomposition.

27. Regarding claim 23, Cho discloses each of the emitters being formed by thiolizing a pre-synthesized carbon nano-tube and applying thereto an Au-S chemical composition process.

28. Regarding claim 24, Cho discloses each of the emitters being formed by performing an electrodephoresis process on a pre-synthesized carbon nano-structure.

29. Regarding claim 25, Figure 1 of Cho shows more than one emitter formed in each of the second sub-micro holes.

30. Regarding independent claim 26, Figures 1-8 of Cho show a method for fabricating an electric field emission device having a triode structure by using an anodic oxidation process comprising the steps of forming a bottom electrode (11) on a supporting substrate (10), the bottom electrode layer being used as a cathode electrode of the device; forming sequentially a gate insulating layer (12), a gate electrode layer (13), and an anode insulating layer (15) and an aluminum layer (19) on the bottom electrode layer; forming a plurality of first sub-micro holes in an alumina layer by performing an anodic oxidation process on the aluminum layer, thereby transforming the aluminum layer into the alumina layer; etching a barrier layer of the alumina layer, the anode insulating layer and the gate electrode layer, thereby a surface of the gate insulating layer being exposed through the first sub-micro holes; forming a plurality of second sub-micro holes in the gate insulating layer, thereby each of the first sub-micro holes connecting to a corresponding one of the second sub-micro holes; removing the alumina layer; forming an emitter (23) for emitting electrons in a high electric field in each of the second sub-micro holes; and forming a top electrode layer (Fig. 8) for

hermetically sealing the device on the alumina layer in a vacuum, the top electrode layer being used as an anode of the device.

31. Regarding claim 27, Cho discloses the anodic oxidation process being performed by using an electrolyte selected from a group consisting of oxalic acid, sulfuric acid, phosphoric acid, and chromic acid.

32. Regarding claim 28, Cho discloses the alumina layer being removed by dipping the alumina layer in a solution of phosphoric acid or a mixed solution of phosphoric acid and chromic acid.

33. Regarding claim 29, Cho discloses each of the emitters being formed by growing metal from a bottom of each of the second sub-micro holes.

34. Regarding claim 30, Cho discloses the metal being grown by applying DC or AC voltage or voltage pulse to a solution of metal sulfate, metal nitrate, or metal chloride.

35. Regarding claim 31, Cho discloses the metal being grown by using a solution of metal sulfate, metal nitrate, or metal chloride after chemically activating a surface of the bottom.

36. Regarding claim 32, Cho discloses each of the emitters being formed by attaching a metal to a bottom of each of the second sub-micro holes.

37. Regarding claim 33, Cho discloses each of the emitters being formed by forming a carbon nano-structure on a bottom of each of the second sub-micro holes.

38. Regarding claim 34, Cho discloses the carbon nano-structure being one of carbon nano-tube, carbon nano-fiber, amorphous carbon, and carbon nano-particle, which are composed by using a thermal decomposition.

39. Regarding claim 35, Cho discloses the thermal decomposition being performed by thermally decomposing a gas mixture of hydrocarbon, carbon monoxide, and hydrogen at 200-800°C.

40. Regarding claim 36, Cho discloses the carbon nano-structure being one of carbon nano-tube, carbon nano-fiber, amorphous carbon, and carbon nano-particle, which are composed by using a plasma decomposition.

41. Regarding claim 37, Cho discloses each of the emitters being formed by thiolizing a pre-synthesized carbon nano-tube and applying thereto an Au-S chemical composition process.

42. Regarding claim 38, Cho discloses each of the emitters being formed by performing an electrodephoresis process on a pre-synthesized carbon nano-structure.

43. Regarding claim 39, Figure 1 of Cho shows more than one emitter formed in each of the second sub-micro holes.

Response to Arguments

44. Applicant's arguments filed 04 January 2008 have been fully considered but they are not persuasive.

45. Applicant notes that claims 1 and 11 recite the alumina layer being formed on every gate electrode layer. Independent claim 1 recites "an alumina layer formed on the gate electrode layer..." in line 11 of the claim. The Examiner notes that this recitation does not require the alumina layer to be formed on every gate electrode layer. Independent claim 11 recites "forming sequentially a gate insulating layer, a gate electrode layer and an aluminum layer on the bottom electrode layer; forming a plurality

of first sub-micro holes in an alumina layer by performing an anodic oxidation process on the aluminum layer, thereby transforming the aluminum layer into the alumina layer" in lines 5-9 of the claim. The Examiner notes that this recitation also does not require the alumina layer to be formed on every gate electrode.

46. Applicant also mentions that claim 6 and 26 recite the anode insulating layer being formed on every gate electrode layer (no void space on the gate electrode layer). The Examiner notes that independent claim 6 recites "an anode insulating layer formed on the gate electrode layer" in line 11 of the claim. The Examiner notes that this recitation does not require the anode insulating layer to be formed on every gate electrode layer, such that there is no void space on the gate electrode layer. Independent claim 26 recites "forming sequentially a gate insulating layer, a gate electrode layer, an anode insulating layer and an aluminum layer on the bottom electrode layer" in lines 5-6 of the claim. The Examiner notes that this recitation does not require the anode insulating layer to be formed on every gate electrode layer, such that there is no void space on the gate electrode layer.

47. In response to applicant's argument that Cho fails to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the shapes and functions of the spacer; layer thicknesses) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

48. Applicant also notes that according to independent claims 1, 6, 11, and 26, one micro hole is surrounded by the bottom electrode layer, the gate insulating layer, the gate electrode layer, the alumina layer and the top electrode layer, and thus, micro holes are formed separately from each other. The Examiner notes that the above features are not recited in the claims, and thus, do not need to be taught in the prior art reference of Cho.

Conclusion

49. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

50. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quarterman whose telephone number is (571)272-2461. The examiner can normally be reached on M-TH (7-5:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Minh-Toan Ton can be reached on (571) 272-2303. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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Examiner
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14 April 2008

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